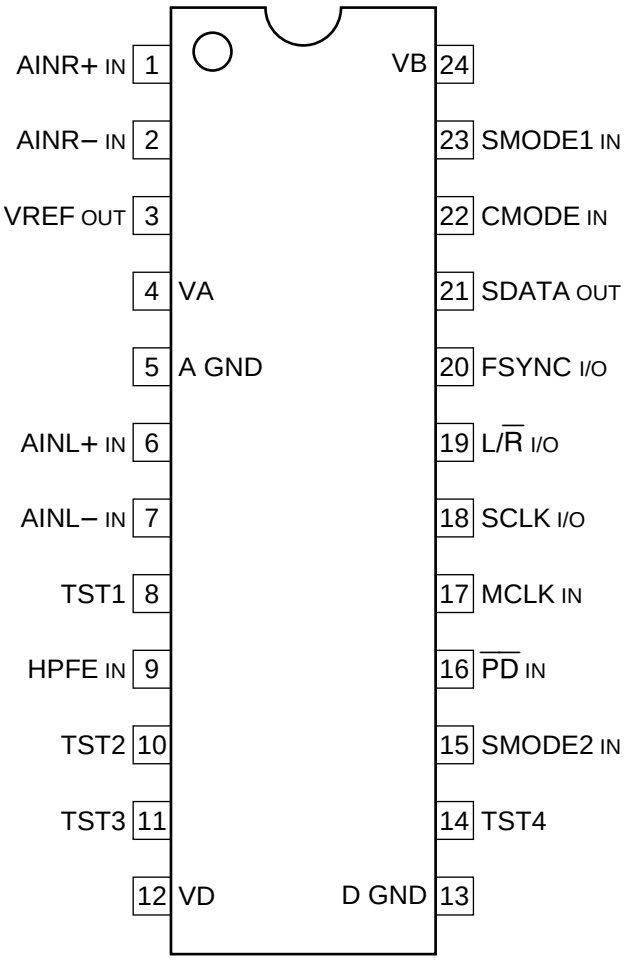
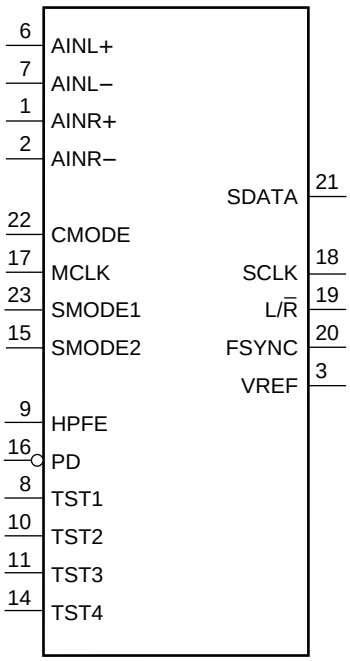
C-MOS 20-BIT A/D CONVERTER

—TOP VIEW—





INPUT

AINL+ : CHANNEL L ANALOG POSITIVE INPUT
AINL− : CHANNEL L ANALOG NEGATIVE INPUT
AINR+ : CHANNEL R ANALOG POSITIVE INPUT
AINR− : CHANNEL R ANALOG NEGATIVE INPUT
CMODE : MASTER CLOCK SELECT
(L : MCLK = 256 fs)
(H : MCLK = 384 fs)
HPFE : HIGH PASS FILTER ENABLE
(L : OFF)
(H : ON)
MCLK : MASTER CLOCK
(CMODE = H : 384 fs)
(CMODE = L : 256 fs)
$\overline{PD}$: POWER DOWN
(L : POWER DOWN MODE)
SMODE1, SMODE2 : INTERFACE CLOCK SELECT

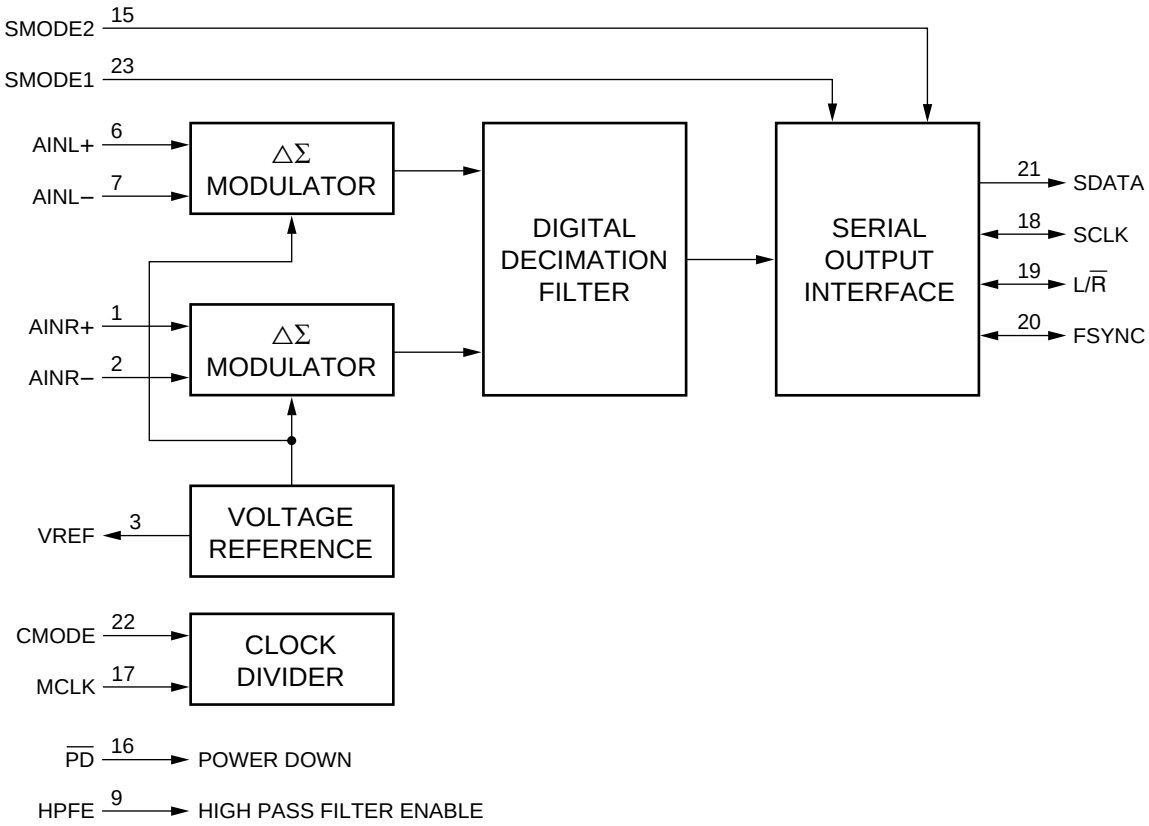
SMODE1	SMODE2	MODE	LRCK
L	L	SUB MODE	H/L
H	L	MASTER MODE	H/L
L	H	SUB MODE	L/H
H	H	MASTER MODE	L/H

OUTPUT

SDATA : SERIAL DATA
VREF : REFERENCE VOLTAGE

INPUT/OUTPUT

FSYNC : FRAME SYNC CLOCK
L/$\overline{R}$: INPUT CHANNEL SELECT
(SUB MODE : fs CLK INPUT)
(MASTER MODE : fs CLK OUTPUT)
SCLK : SERIAL DATA CLOCK
(SUB MODE : 64 fs CLK INPUT)
(MASTER MODE : 64 fs CLK OUTPUT)


SMODE2
15
SMODE1
23
AINL+
6
AINL–
7
△Σ
MODULATOR
AINR+
1
AINR–
2
△Σ
MODULATOR
DIGITAL
DECIMATION
FILTER
SERIAL
OUTPUT
INTERFACE
21
SDATA
18
SCLK
19
L/R
20
FSYNC
VREF
3
VOLTAGE
REFERENCE
CMODE
22
MCLK
17
CLOCK
DIVIDER
PD
16
POWER DOWN
HPFE
9
HIGH PASS FILTER ENABLE